AMENDMENTS TO THE CLAIMS

The following listing of claims will replace all prior versions and listings of claims in the application.

LISTING OF CLAIMS

1-42. (Cancelled)

43. (currently amended) A self-programming, mixed-mode chip for estimation, prediction and control, comprising:

an array of synaptic cells which are interconnected to form a feedforward neural network, wherein each synaptic cell includes:

a learning electrical circuit operable to update a local weight according to an update rule and store the local weight in a capacitor;

a digital memory arranged in parallel with the capacitor ~~and~~ where the digital memory is operable to store the local weight in a digital form; and

a processing electrical circuit comprised of a one-dimensional multiplier which is operable to process a component of an analog input signal in accordance with the local weight stored in the digital memory.

44. (previously presented) The mixed-mode chip of Claim 43, wherein each column of synaptic cells in the array of synaptic cells represents a neuron in the neural network.

45. (previously presented) The mixed-mode chip of Claim 43, further comprising an array of control cells positioned adjacent to the array of synaptic cells, where each control cell controls conversion of the local weight from an analog form to a digital form for a row of synaptic cells in the array of synaptic cells.

46. (previously presented) The mixed-mode chip of Claim 45, wherein the control cells operate synchronously with each other to control conversion.

47. (previously presented) The mixed-mode chip of Claim 45, wherein each control cell includes a multiplexer configured to select a synaptic cell in a given row of synaptic cells and an analog-to-digital converter.

48. (previously presented) The mixed-mode chip of Claim 47, wherein the analog-to-digital converter for a given row of synaptic cells is interconnected to each synaptic cell in the given row of synaptic cells.

49. (cancel)

50. (cancel)

51. (previously presented) The mixed-mode chip of Claim 43, further comprising a switch interposed between the processing circuit and the digital memory for selectively enabling use of the digital memory.

52. (previously presented) The mixed-mode chip of Claim 43, further comprising a switch interposed between the processing circuit and the learning circuit for selectively enabling use of the learning circuit.

53. (previously presented) The mixed-mode chip of Claim 43, further comprising a switch interposed between the processing circuit, the learning circuit and the digital memory for selectively enabling the use of either the learning circuit or the digital memory by the processing circuit.

54. (previously presented) The mixed-mode chip of Claim 43, wherein the learning circuit is comprised of a one-dimensional multiplier for implementing the update rule.

55. (previously presented) The mixed mode chip of Claim 43, wherein the learning circuit is configured to receive an error signal indicative of a difference between an output signal and a target output signal.

56. (previously presented) The mixed-mode chip of Claim 55, further comprising multiple arrays of synaptic cells which are interconnected to form a multi-layer neural network.

57. (previously presented) The mixed-mode chip of Claim 56, wherein the learning circuit further comprises a second multiplier configured to receive the error signal and generates a feedback propagation error signal for a previous layer in the multi-layer neural network.

58. (previously presented) The mixed-mode chip of Claim 43, wherein the digital memory is implemented using flip-flops.

59. (previously presented) The mixed-mode chip of Claim 43, further comprising a digital-to-analog converter interposed between the processing circuit and the digital memory in each synaptic cell.

60. (previously presented) The mixed-mode chip of Claim 43, wherein each processing circuit in a column of synaptic cells outputs a component of a weighted sum.

61. (previously presented) The mixed-mode chip of Claim 43, wherein an output of each multiplier in a column of synaptic cells is interconnected to form a weighted sum.

62. (currently amended) A self-programming, mixed-mode chip for estimation, prediction and control, comprising:

an array of synaptic cells which are interconnected to form a feedforward neural network and configured to receive an analog input signal indicative of a biological cell measurement and to model a process of the biological cell, wherein each synaptic cell includes:

a learning electrical circuit operable to update a local weight according to an update rule and store the local weight in a capacitor;

a digital memory arranged in parallel with the capacitor ~~and~~ where the digital memory is operable to store the local weight in a digital form; and

a processing electrical circuit comprised of a one-dimensional multiplier which is operable to process a component of the analog input signal in accordance with the local weight stored in the digital memory.

63. (previously presented) The mixed-mode chip of Claim 62, wherein each column of synaptic cells in the array of synaptic cells represents a neuron in the neural network.

64. (previously presented) The mixed-mode chip of Claim 62, further comprising an array of control cells positioned adjacent to the array of synaptic cells, where each control cell controls conversion of the local weight from an analog form to a digital form for a row of synaptic cells in the array of synaptic cells.

65. (previously presented) The mixed-mode chip of Claim 64, wherein the control cells operate synchronously with each other to control conversion.

66. (previously presented) The mixed-mode chip of Claim 64, wherein each control cell includes a multiplexer configured to select a synaptic cell in a given row of synaptic cells and an analog-to-digital converter.

67. (previously presented) The mixed-mode chip of Claim 66, wherein the analog-to-digital converter for a given row of synaptic cells is interconnected to each synaptic cell in the given row of synaptic cells.

68. (cancel)

69. (cancel)

70. (previously presented) The mixed-mode chip of Claim 62, further comprising a switch interposed between the processing circuit and the digital memory for selectively enabling use of the digital memory.

71. (previously presented) The mixed-mode chip of Claim 62, further comprising a switch interposed between the processing circuit and the learning circuit for selectively enabling use of the learning circuit.

72. (previously presented) The mixed-mode chip of Claim 62, further comprising a switch interposed between the processing circuit, the learning circuit and the digital memory for selectively enabling the use of either the learning circuit or the digital memory by the processing circuit.

73. (previously presented) The mixed-mode chip of Claim 62, wherein the learning circuit is comprised of a one-dimensional multiplier for implementing the update rule.

74. (previously presented) The mixed mode chip of Claim 62, wherein the learning circuit is configured to receive an error signal indicative of a difference between an output signal and a target output signal.

75. (previously presented) The mixed-mode chip of Claim 74, further comprising multiple arrays of synaptic cells which are interconnected to form a multi-layer neural network.

76. (previously presented) The mixed-mode chip of Claim 75, wherein the learning circuit further comprises a second multiplier configured to receive the error signal and generates a feedback propagation error signal for a previous layer in the multi-layer neural network.

77. (previously presented) The mixed-mode chip of Claim 62, wherein the digital memory is implemented using flip-flops.

78. (previously presented) The mixed-mode chip of Claim 62, further comprising a digital-to-analog converter interposed between the processing circuit and the digital memory in each synaptic cell.

79. (previously presented) The mixed-mode chip of Claim 62, wherein each processing circuit in a column of synaptic cells outputs a component of a weighted sum.

80. (previously presented) The mixed-mode chip of Claim 62, wherein an output of each multiplier in a column of synaptic cells is interconnected to form a weighted sum.

81. (currently amended) A self-programming, mixed-mode chip for estimation, prediction and control, comprising:

an array of synaptic cells which are interconnected to form a feedforward neural network, wherein each synaptic cell includes:

a learning electrical circuit operable to update a local weight according to an update rule and store the local weight in a capacitor, wherein the learning circuit is comprised of a one-dimensional multiplier for implementing the update rule, and is configured to receive an error signal indicative of a difference between an output signal and a target output signal;

a digital memory arranged in parallel with the capacitor ~~and~~ where the digital memory is operable to store the local weight in a digital form, wherein the digital memory is implemented using flip-flops;

a processing electrical circuit comprised of a one-dimensional multiplier which is operable to process a component of an analog input signal in accordance with the local weight stored in the digital memory;

a switch interposed between the processing circuit, the learning circuit, and the digital memory for selectively enabling the use of either the learning circuit or the digital memory by the processing circuit;

a digital-to-analog converter interposed between the processing circuit and the digital memory in each synaptic cell.

82. (previously presented) The mixed-mode chip of Claim 81, further comprising multiple arrays of synaptic cells which are interconnected to form a multi-layer neural network, wherein the learning circuit further comprises a second multiplier configured to receive the error signal and generates a feedback propagation error signal for a previous layer in the multi-layer neural network.

83. (previously presented) The mixed-mode chip of Claim 81, wherein an output of each multiplier in a column of synaptic cells is interconnected to form a weighted sum, and each processing circuit in a column of synaptic cells outputs a component of the weighted sum.

84. (previously presented) The mixed-mode chip of Claim 81, wherein each column of synaptic cells in the array of synaptic cells represents a neuron in the neural network.

85. (previously presented) The mixed-mode chip of Claim 81, further comprising an array of control cells positioned adjacent to the array of synaptic cells, where each control cell controls conversion of the local weight from an analog form to a digital form for a row of synaptic cells in the array of synaptic cells.

86. (previously presented) The mixed-mode chip of Claim 85, wherein the control cells operate synchronously with each other to control conversion.

87. (previously presented) The mixed-mode chip of Claim 85, wherein each control cell includes a multiplexer configured to select a synaptic cell in a given row of synaptic cells and an analog-to-digital converter.

88. (previously presented) The mixed-mode chip of Claim 87, wherein the analog-to-digital converter for a given row of synaptic cells is interconnected to each synaptic cell in the given row of synaptic cells.

89. (cancel)

90. (cancel)